**CS224**

**Section No: 6**

**Spring 2021**

**Lab No: 6**

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**Question 1:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **No.** | **Cache Size KB** | **N**  **way cache** | **Word Size in bits** | **Block size (no. of words)** | **No. of Sets** | **Tag Size in bits** | **Index Size (Set No.) in bits** | **Word Block Offset Size in bits1** | **Byte Offset Size in bits2** | **Block Replacement Policy Needed (Yes/No)** |
| 1 | 8 | 1 | 8 | 8 | 210 | 19 | 10 | 3 | 0 | No |
| 2 | 8 | 2 | 16 | 8 | 28 | 20 | 8 | 3 | 1 | Yes |
| 3 | 8 | 4 | 16 | 4 | 28 | 21 | 8 | 2 | 1 | Yes |
| 4 | 8 | Full | 16 | 4 | 20 | 29 | 0 | 2 | 1 | Yes |
| 9 | 32 | 1 | 16 | 2 | 213 | 17 | 13 | 1 | 1 | No |
| 10 | 32 | 2 | 16 | 2 | 212 | 18 | 12 | 1 | 1 | Yes |
| 11 | 32 | 4 | 8 | 8 | 210 | 19 | 10 | 3 | 0 | Yes |
| 12 | 32 | Full | 8 | 8 | 20 | 29 | 0 | 3 | 0 | Yes |

**Question 2:**

**a)**  **Type Of Miss**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Instruction** | **Iteration No.** | | | | |
| **1** | **2** | **3** | **4** | **5** |
| lw $t1, 0xA4($0) | Compulsory | Hit | Hit | Hit | Hit |
| lw $t2, 0xA8($0) | Hit | Hit | Hit | Hit | Hit |
| lw $t3, 0xAC($0) | Hit | Hit | Hit | Hit | Hit |

**b)**

**Cache Representation**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
|  | **V** | **Tag** | **Data** | **Data** | **Data** | **Data** |
| Set 1 | 1 bit | 27 bits | 32 bits | 32 bits | 32 bits | 32 bits |
| Set 0 | 1 bit | 27 bits | 32 bits | 32 bits | 32 bits | 32 bits |

Cache Capacity = 8 words

Block Size = 4 words

N = 1

Block Offset = log24 = 2 bits

Byte Offset = log24 = 2 bits

Set Size = 8/4 = 2/1 = 2

Set = 1 bit

Tag = 32 – (1 + 2 + 2) = 27 bits

Total Cache Memory = (1 + 27 + 32 + 32 +32 + 32 ) x 2 = 312 bits

**c) Required Hardware**

One 4x1 Mux for selecting the word in the desired block.

One Equality Comparator for comparing the tags

One AND Gate to determine the hit

**Question 3:**

**a) Type Of Miss**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Instruction** | **Iteration No.** | | | | |
| **1** | **2** | **3** | **4** | **5** |
| lw $t1, 0xA4($0) | Compulsory | Capacity | Capacity | Capacity | Capacity |
| lw $t2, 0xA8($0) | Compulsory | Capacity | Capacity | Capacity | Capacity |
| lw $t3, 0xAC($0) | Capacity | Capacity | Capacity | Capacity | Capacity |

**b)**

**Cache Representation**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **V** | **Tag** | **Data** | **V** | **Tag** | **Data** |
| 1 bit | 30 bits | 32 bits | 1 bit | 30 bits | 32 bits |

Cache Capacity = 2 words

Block Size = 1 word

N = 2

Block Offset = log21 = 0 bit

Byte Offset = log24 = 2 bits

Set Size = 2/1 = 2/2 = 1

Set = 0 bit

Tag = 32 – (2) = 30 bits

Total Cache Memory = (1 + 30 + 32) x 2 = 126 bits

**c) Required Hardware**

One 2x1 Mux for selecting the way in the desired block

Two Equality Comparator for comparing the tags

Two AND Gate

One OR Gate to determine the hit